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Abstract
Engineering designs of high-frequency products are on the rise. In accompany to the development of highly-performed electronic products of such kind, designers often stress the importance of power-saving, compatibility, and electronic magnetic interference prevention. Asynchronous circuit is the solution to the fulfillment of the mentioned design requirement, which provides features such as low power dissipation, feasibility of modularization, low EMI and so on. Moreover, asynchronous circuit design has become the trend of the future alternative design technology as well as the extension in educational training. Unfortunately, availability of the design tools today is not sufficient and complete. Another difficulty for promoting the design flow of the design is its complexity, which is a setback when promoting the utilization of the design tools, and its corresponding applications.
One major step in the design process is the methodology for verifying the designed circuits. Currently, we could verify the circuit by performing various tests on the circuit layout to the actual wafer; but we can also verify the design by running the simulation software to verify. However, there is still a gap between the accuracy of data obtained by the featured simulation software and by the actual circuit. Another inefficiency is the designers must wait long period of time for the chip to return from fabrication in order to go on to the verification process. Timing control for obtaining higher reliable simulated data is also hard to manipulate. Consequently, we decide to design the circuit by the use of FPGA board, which is advantageous for reducing the development time, and cost to repeatedly over-writing instead of chip fabrication.
The asynchronous extended burst-mode (XBM) controller design described in this thesis is based on the synthesis tool named “3D”, which is developed by K.Y. Yun, a UC San Diego professor. The tool“3D”allows us to implement our design by programming hardware description language (HDL) and synthesizing the HDL coding in the formation of datapath module and delay element in order to achieving circuit realization of self-timed datapath module. Furthermore, we combine the controller module and the self-timed datapath module to create a complete asynchronous circuit, load the circuit to a well-established test platform, and measure to collect valid data associating with the interface of the platform.
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